

REMARKS/ARGUMENTS

Applicant would like to thank the Examiner for the thorough review of the present application. As discussed in detail below, the present claims in the present application include recitations that patentably distinguish the claimed invention over the cited references, taken individually or in combination. Based upon the following remarks, Applicant respectfully requests reconsideration of the present application and allowance of the pending claims.

The Present Invention

The invention provides for an imaging device and associated methods for simultaneously capturing image data and image display update. The invention implements first and second buffers (i.e., dual or double buffers) that are capable of capturing an image in one buffer while a second buffer displays the image on an associated imaging device display. This provides for overall efficiency in the use of the device, in that the imaging device and method provide the capability to capture and display every frame that the imager processes. Such a device benefits from real-time aiming, capture and display of image data.

The invention *requires, per amended Claim 1*, that the two image capture buffers be included within a single memory module and that this memory module be accessible to the Central Processing Unit (CPU). The first image capture buffer is *required, per amended Claim 1*, to temporarily store first-in time captured image data prior to displaying the first-in-time image data and the second image capture buffer is *required, per amended Claim 1*, to temporarily store second-in-time captured image data prior to displaying second-in-time image data.

Amendments to the Claims

Claim 1 has been amended to specifically state that the first and second image capture buffers are accessible to the CPU. As will be discussed below, we believe that by more accurately defining the buffers in terms of their accessibility to the CPU distinguishes our

invention from the teachings of Shand. Accessibility by the CPU to each of the double buffers is required by our invention so that data can be drawn quickly on the associated display.

35 U.S.C. § 103 (a) Rejection

Roth '528 Patent in view of the Shand '159 Patent

Claims 1-6, stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over the Roth '528 patent in view of the Shand '159 patent. Specifically, the Examiner asserts that the Roth '528 patent and the Shand '159 patent teach the following elements of Claim 1:

1. An imaging device for simultaneous image capture and image display updating
(*Roth '528 at Fig. 1, Col. 7, lines 24-27; Col. 16, lines 48-66; Fig. 22, Col. 25 lines 2-12*)
the device comprising:

an imager (*Roth '528 at Column 3, lines 45-67*) for capturing image data upon aiming the imager at an image (*Roth '528 at Column 7, lines 22-38*);

a central processing unit (CPU) that is in communication with the imager and issues commands to capture image data (*Roth '528 at Column 4, lines 40-55*);

a direct memory access module in communication with the imager and the CPU that executes the commands to capture image data (*Shand '159 at Column 4, lines 1-5; 43-55*);
and

a memory module in communication with the CPU and the DMA module, the memory module including a first image capture buffer that temporarily stores first-in-time captured image data prior to displaying first-in-time image data and a second image capture buffer that temporarily stores second-in-time captured image data prior to displaying second-in-time image data (*Shand '159 at Col. 2, lines 5-25; Fig. 1, element 300; Col. 3, lines 19-22 (image buffer), 30-32 (frame buffer for storing pixels of a displayed image); 35-40, line 55 – Col. 4 line 5; Col. 5, lines 5-64, double buffers; Col. 4 lines 63- Col. 5, line 12*).

The applicant respectfully disagrees with the Examiner's rejection of the Claims under 35 U.S.C. § 103 (a) for the following reasons.

The Shand '159 Patent Does Not Teach or Suggest a Memory Module that includes First and Second Buffers that Store "First-In-Time" and "Second-In-Time Data" and are Accessible to the CPU.

Claim 1 of the present invention, as amended, requires that imaging device for simultaneous image capture and image display updating include a memory module. The memory module must include both first and second image capture buffers. Both the first and second image capture buffers must be accessible to the CPU. Additionally, the image capture buffers must, respectively, temporarily store first-in-time captured image data and second-in-time captured image data prior to displaying first-in-time image data and second-in-time image data.

The Shand '159 patent addresses the problem of relieving the CPU of the burden of reformatting image data. In doing so, the Shand invention allows the device to quickly process image data whose format does not match the frame buffer in memory. As the examiner is aware, the Shand '159 patent does not provide for a teaching of simultaneous image capture and image display, i.e., having the CPU draw from one buffer while an image is being captured into another buffer. Therefore, the buffers that are taught in the Shand '159 patent are categorically different from the buffers claimed in the present invention, in that, they are either located in different portions of the device, not accessible to the CPU or do not store first-in-time captured image data and second-in-time captured image data prior to displaying first-in-time image data and second-in-time image data.

The Shand '159 patent teaches several different types of double buffers, however; no one set of buffers meet all of the requirements of Claim 1. To verify this statement, we refer you to the sections within the Shand '159 patent that were cited in the Office Action.

Referring to Column 2, line 5-25. In the Invention Summary portion of the Shand '159 patent it teaches a single buffer (called "first buffer"), furthermore, this portion of the patent provides no teaching that the CPU has access to the buffer.

Referring to Figure 1, element 300. While the Shand '159 patent teaches double buffers within Configurable Interface 300, no teaching is provided that the CPU has access to both double buffers. The teaching of Figure 1, element 300 is limited to a teaching that the Configurable Interface communicates with the processor 200. However, as further discussion will indicate, the Shand '159 does not provide a teaching that both of the double buffers within the Configurable Interface 300 are accessible to the CPU.

Referring to Column 3, line 19 - 22. This portion of the Shand '159 patent refers to an image buffer portion 221 of the memory 220. Additionally, this portion of the patent teaches that the CPU 210 has access to the image buffer portion. However, no teaching is provided that the memory includes *two* image capture buffers.

Referring to Column 3, line 30 - 32. This portion of the Shand '159 refers to a frame buffer 241. However, as Figure 2 illustrates, the frame buffer is located in the I/O controllers 240, i.e., not in memory, 220. Once again, no teaching is provided that the memory includes *two* image buffers.

Referring to Column 5, line 5 - 64. While this portion of the Shand '159 patent makes reference to double buffers none of the double buffer sets that are taught either (1) store "first-in-time" and "second-in-time" data or (2) located in memory and accessible by the CPU.

At Column 5, lines 5-12, the Shand '159 patent teaches two buffers that are in memory, the first is buffer 241 and the existence of the second can be implied by the phrase, "The least significant portions can be stored elsewhere in memory 220...". In this instance, both buffers are located in memory and the CPU has access to them. However, each buffer stores only a portion of the same image. Buffer 241 stores the most significant portion of the image while the implied

buffer stores the least significant portion of the image. The invention taught by the Shand '159 patent takes the input pixel stream and separates it into two stream transport channels (Column 4, lines 62 to Column 5, line 4). Each buffer stores data from one of these channels. Thus, these buffers contain data that is generated at the "same time" because; the buffers contain data separated from a single input pixel stream. By comparison, Claim 1 of the present invention requires one buffer in memory that stores, "first-in-time image data" and a second buffer in memory that stores "second-in-time image data".

At Column 5, lines 27-32, two sets of double buffers are described; one set is 521 and 522 and the other set is 523 and 524. At Column 5, lines 57-62, two sets of double buffers are described; one set is 721 and 722 and the other is 723 and 724 (Note that Fig. 5, 500 is a particular implementation of the more general diagram Fig. 3, 300). Both of these sets are located within the FPGA and the CPU does not have access to the buffers.

All of these sets of buffers are located within the FPGA, and not in memory. Column 3, line 55 states, "In a preferred embodiment of the invention, the interface 300 uses field programmable gate array (FPGA)." Also, Column 4, line 23 says, "... under the direction of the DMA controller 330, the words 305 are transported to the image buffer 221 of the memory 220...". Thus, since the Shand '159 patent teaches that the data requires transfer from the double buffers *into* memory it be logically concluded that these double buffers are not memory. By comparison, Claim 1 of the present invention requires the first and second image capture buffers to be included within the memory module.

Additionally, the Shand '159 patent does not teach that the CPU has access to the data stored in the sets of buffers. This is evident by the fact that the patent teaches only one data path between the bus 250, and the buffers, 521-524 or 721-724. The one path that is taught is through the DMA controller (see the discussion at Column 4, line 22-27). It is well known by those of ordinary skill in the art, that DMA controllers transfer data from digital electronic devices into memory. It is also well known by those of ordinary skill in the art that DMA controllers do not permit CPUs to access data located in buffers outside of memory. In order for the CPU to access

buffers 521-524 or buffers 721-724, some mechanism would have to exist to facilitate this access. Shand does not teach nor suggest such a mechanism. Therefore, the logical conclusion that can be drawn from the lack of such a mechanism in Shand's teachings is that it is not possible for the CPU to access the double buffers. By comparison, amended Claim 1 of the present invention requires that the first and second image capture buffers be accessible to the CPU. As previously, discussed this accessibility is needed so that the CPU can rapidly provide an image on an associated display.

At Column 5, lines 40-42 refer to buffers 321 and 322 in Figure 6. The Shand '159 patent provides no teaching or suggestion that these buffers are located in memory. Additionally, the Shand '159 patent provides no teaching that these buffers are accessible by the CPU. Additionally, the Shand '159 patent teaches that these buffers store data that was generated at the same time, i.e., not first-in-time data and second-in-time data, (see Column 5, lines 39-43).

Referring to Column 4, line 63 to Column 5, line 12. This section of the patent refers to the same buffers discussed, *infra* in relation to Column 5, lines 5-12. Specifically, frame buffer 241 and the existence of a second implied buffer. These buffers are located in memory but they do not store "first-in-time" and "second-in-time" data. They store data that was generated at the "same time."

Therefore, Applicant asserts that Claim 1 directed towards an imaging device for simultaneous image capture and image display updating is distinguishable from the teachings of Shand '159 and, in particular the memory module of Claim 1 is distinguishable from the teachings of Shand '159. Hence, the Applicant asserts that Claim 1 cannot be obviated by the combination of Roth '528 in view of Shand '159, because Shand '159 does not teach the memory module element as required by Claim 1.

Claims 2-6 are dependent claims that depend from Claim 1. These claims add further limitations to Claim 1. Therefore, since the Applicant believes that Claim 1 is patentable, in

view of the amendment and the remarks above, the dependent Claims 2-6 must also be deemed patentable, as a matter of law.

The Shand '159 Patent Does Not Provide a Motivation to Combine the Teachings therein with the Teachings described in the Roth '528 Patent.

Aside from the convincing argument presented above, the Applicant does not believe that Shand '159 provides the requisite motivation, required by 35 U.S.C. 103 (a), to combine the teachings in the Shand '159 patent with the teachings in the Roth '528 patent to obviate the present invention.

The Shand '158 reference is motivated by the need to relieve the CPU of the burden of reformatting image data. The present invention does not concern itself with reformatting image data, but rather addresses the need to allow the CPU to draw streaming image data on the display more quickly.

The Examiner relies on the following portions of the Shand patent to provide motivation for combining. According to the Examiner, Column 1, lines 30-37 provides motivation in that it the Shand '158 patent "enables reading high precision images as fast as possible. According to this portion of the Shand '158 patent the motivation is, "... adapt externally produced image signals having a higher precision than eight bits to conventional frame buffers." The applicant fails to appreciate how this motivation can be equated with enabling reading of high precision images as fast as possible.

At Column 1, lines 38- 48, the Examiner states that motivation is provided, in that, the Shand '158 patent addresses enabling real-time software format processing of image data. The present invention does not address reformatting image data.

At Column 4, line 38 – 42, the Examiner states that motivation is provided, in that, the Shand '158 patent addresses double buffers that enable receiving pixel data from a converter.

The present invention does not implement a converter because the present invention does not reformat data.

Therefore, since the Applicant asserts that the Shand '158 patent provides no motivation for combining the teachings therein with the teachings in the Roth '528 patent, the Examiner has not met the burden of demonstrating the requisite motivation that 35 U.S.C. 103 (a) requires.

35 U.S.C. § 102 (b) Rejection

Roth '528 Patent

Claim 7 stands rejected under 35 U.S.C. § 102 (b) as being anticipated by the Roth '528 patent. Specifically, the Examiner asserts that the Roth '528 patent teaches all of elements of Claim 7:

A method for simultaneous image capture and image display in an imaging device, the method comprising the steps of:

capturing first-in-time image data to a first image capture buffer that is in communication with an imager;

capturing second-in-time image data to a second image capture buffer that is in communication with an imager; and

displaying the first-in-time image data on a display while the image device captures the second-in time image data to the second image capture buffer.

The Examiner directs the Applicant to the following portions of the Roth '528 patent: video Ram and label image data, Column 13, lines 40-67, gain values, Column 4, lines 12-14, 37-55, the second memory includes a bin...to each possible intensity level; Column 16, lines 28-35; Figures 11, Column 17, lines 35-37; Column 19, lines 46-Column 20, line 6, three distinct fields or exposures; data buffers, Column 20, lines 12-24.

The applicant respectfully disagrees with the Examiner's rejection of the Claims under 35 U.S.C. § 102 (b) for the following reasons.

The Roth '528 Patent Fails to Disclose Capturing First-In-Time Image Data to a First Image Capture Buffer and Capturing Second-In-Time Image Data to a Second Image Capture Buffer.

The Applicant fails to appreciate any teaching in Roth of double buffers that capture "first-in-time" and "second-in-time" image data. Column 4, lines 40-55 describe a method for generating a histogram to evaluate the intensity of an image. The method includes first and second memories. The first memory defines test bits and the second memory includes a bin corresponding to each possible intensity level of the pixels. The second memory stores the histogram. Applicant respectfully asserts that these memories are not image capture buffers, which capture "first-in-time" and "second-in-time" images. By definition, a buffer will characteristically change over time, in terms of the data that it stores. In the Roth '528 patent the first memory stores bits and the teaching implies that memory containing the bits will never change. If the memory does not change, it cannot be stated that the memory stores "first-in-time" data, such as in an image capture buffer.

Additionally, Column 4, lines 37 - 55 of the Roth '528 patent describes how a histogram is generated. Column 20, line 21 to Column 21, line 56 of the Roth '528 patent elaborates on how the histogram is generated. Column 4, lines 48 - 50 of the Roth '528 patent describes how a first memory containing test bits is used to select which bin in the histogram will be incremented. Column 20, lines 32 - 48 of the Roth '528 patent describes how a HIT TABLE containing HIT BITS is used to select which bins in a histogram will be incremented. The applicant infers that that the HIT TABLE is the same as the first memory and the HIT BITS are the same as the test bits. As discussed above the test bits, i.e., HIT BITS are permanently stored in the HIT TABLE of the first memory. Applicant fails to appreciate how the HIT TABLE and the HIT BITS equate to image capture buffers that capture "first-in-time" image data.

Moreover, at Column 20, lines 32-33 the Roth '528 patent states that the HIT TABLE is stored in EPROM. EPROMs are typically written once. Once written, it is not possible to change the data in them without going through a lengthy erase cycle. The fact that the HIT TABLE, or first memory is stored in EPROM and Roth does not describe a mechanism for erasing the EPROM, is a strong indication that Roth did not intend for this memory to change, much less store "first-in-time" image data.

If the Examiner believes that other portions of the Roth '528 patent specifically teach the required steps of Claim 7, the Applicant respectfully asks that the Examiner specifically state which portions of the Roth '528 teaching specifically teach each and every step of the method claimed in Claim 7.

Therefore, Applicant asserts that Claim 7 directed towards an a method for simultaneous image capture and image display in an imaging device is distinguishable from the teachings of Roth '528 patent and, in particular does not teach capturing first-in-time image data to a first image capture buffer and capturing second-in-time image data to a second image capture buffer.

Claims 8 - 14 are dependent claims that depend from Claim 7. These claims add further limitations to Claim 7. Therefore, since the Applicant believes that Claim 7 is patentable, in view of the remarks above, the dependent Claims 8-14 must also be deemed patentable, as a matter of law.

35 U.S.C. § 103 (a) Rejection

Roth '528 Patent in view of the Shand '159 Patent

Claims 15- 27, stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over the Roth '528 patent in view of the Shand '159 patent. The Examiner has Independent Claim 15 as being representative of Claim 9, which depends from Independent Claim 7.

The arguments presented in relation to Claim 7 are equally applicable to Claim 15, in that Claim 15 requires the steps of issuing a first command to capture first-in-time image data to a first image capture buffer and issuing a second command to capture second-in-time image data to a second image capture buffer. The Examiner relies solely on the Roth '528 patent as providing a teaching of these steps of the method. As discussed above in relation to our remarks overcoming the 35.U.S.C. § 102 (b) rejection of Claim 7, we find no teaching in the Roth '528 patent of capturing first-in-time image data in a first image capture buffer or capturing second-in-time image data to a second image capture buffer.

Therefore, Applicant asserts that Claim 15 directed towards an a method for simultaneous image capture and image display in an imaging device is distinguishable from the teachings of Roth '528 patent and, in particular does not teach capturing first-in-time image data to a first image capture buffer and capturing second-in-time image data to a second image capture buffer. Hence, the Applicant asserts that Claim 15 can not be obviated by the combination of Roth '528 in view of Shand '159, because Roth '528 does not teach capturing first-in-time image data to a first image capture buffer and capturing second-in-time image data to a second image capture buffer as required by Claim 15.

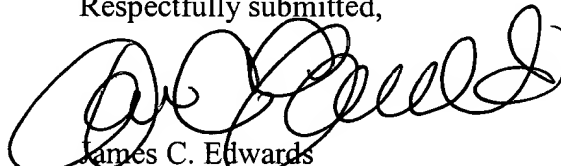
Claims 16-27 are dependent claims that depend from Claim 15. These claims add further limitations to Claim 15. Therefore, since the Applicant believes that Claim 15 is patentable, in view of the remarks above, the dependent Claims 16-27 must also be deemed patentable, as a matter of law.

Conclusion

In view of the proposed amended claims and the remarks submitted above, it is respectfully submitted that the present claims are in condition for immediate allowance. It is therefore respectfully requested that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present invention.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

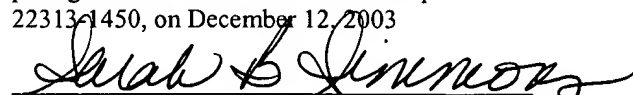


James C. Edwards
Registration No. 44,667

Customer No. 00826
ALSTON & BIRD LLP
Bank of America Plaza
101 South Tryon Street, Suite 4000
Charlotte, NC 28280-4000
Tel Charlotte Office (704) 444-1000
Fax Charlotte Office (704) 444-1111

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 12, 2003



Sarah B. Simmons